												LΤ		

	40	-	-	_	_	-	_	 -		20 m	-	-		33 8	_		200
٠.	5.00	•				• 63			5 E.	PA	П		(E)	1.00		~ I C	•
2.1	1.5	_		36.			95.4	 2.0	2	260		-		47 · W			•

Patent Number:

JP5047666

Publication date:

1993-02-26

Inventor(s):

MATSUMIYA YASUO; others: 02

Applicant(s):

FUJITSU LTD

Requested Patent:

JP5047666

Application Number: JP19910202082 19910813

Priority Number(s):

IPC Classification:

H01L21/205

EC Classification:

EC Classification:

Equivalents:

Abstract

PURPOSE:To alternately perform an ALE and a VPE without exposing a substrate with the atmosphere and without cooling it to the ambient temperature by narrowing between an inner wall of a reaction tube and the substrate on an ALP executing region, extending it on a VPE executing region, and optimizing material gas flowing speeds on the regions. CONSTITUTION: One reaction tube 1 is defined on an ALF optimized region and a VPE optimized region, a substrate 8 is moved to the regions by a susceptor 7, and a compound semiconductor layer of a molecular layer and an atomic layer by a crystalline growth of VPE and an ALF is formed. In this case, the flowing speed of the material gas in the tube 1 is set to a limit value or more for exhibiting a self-limiting effect on the ALE optimized region and to a limit value or less on the VPE optimized region. Thus, a sectional area of the tube 1 is reduced on the ALE optimized region and increased on the VPE optimized region. In this manner, the ALE and the VPE are alternately executed.